## **REMARKS/ARGUMENTS**

Claims 2 and 7 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite; claims 1-11 stand rejected under 35 U.S.C. 102(e) as being anticipated by Ishikawa.

Claims 2 and 7 have been canceled.

Claims 1 and 6 have been amended to include the limitations of sequentially measuring the signals from a reference surface and the surface of the wafer. This sequential measurement is not disclosed in the Ishikawa patent cited by the examiner. In col. 16, lines 56-65, the Ishikawa patent teaches that the signals are obtained simultaneously. The sequential method disclosed in the instant invention offers many advantages, such as simplicity, over the simultaneous system disclosed in the Ishikawa patent. The sequential method of the instant invention in not found in the Ishikawa reference and claims 1 and 6 are allowable under 35 U.S.C. 102(e) over the cited art. Claims 3-5 and 8-9 depend on claims 1 and 6 respectively and therefore contain all the limitations of claims 1 and 6. Therefore, for the reasons stated above, claims 3-5 and 8-9 are also allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including

extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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## **Amendments to the Drawings:**

Formal drawings are filed herewith.